

ABSTRACT

The present invention pertains to an automated method for designing a integrated circuit (IC) design-specific cell, the method includes the steps of receiving a design specification for the design-specific cell, mapping a transistor-level representation of the design-specific cell, wherein the mapping is based on at least one, but perhaps plural design specifications, and evaluating the transistor-level representation of the design-specific cell for satisfaction of the design specification.

10

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